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#17/8-23-02 JR

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant : Ted A. Loxley

Serial No. : 09/490,162 Art Unit: 2812

Filed : January 22, 2000

For: PROCESS AND APPARATUS FOR CLEANING SILICON WAFERS

Examiner : Viktor Simkovic

Docket No. : 104

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APPELLANTS' BRIEF

Sir:

This brief is filed in support of the Notice of Appeal mailed January 17, 2002. The applicable extension of time fee 37 CFR § 1.17(a) (5) is $980. A separate petition requesting the extension and explaining the fee payments is enclosed herewith.

Pursuant to 37 CFR § 1.192, this brief is filed in triplicate and accompanied by a check adequate to cover the requisite fee under 37 CFR § 1.17(c) of $160 for a small entity.

(1) Real party in interest

Ted Albert Loxley, an individual now residing at 236 Tom Corwin Road, Wellston, Ohio.

(2) Related appeals and interferences

There are none.

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(3) Status of claims

There were 31 claims presented in this case prior to the final Office action of October 19, 2001. Of these, claims 1 to 8 were rejected, claims 9 to 13 were allowed, claim 14 was found allowable if rewritten in independent form, apparatus claims 15 to 17 were withdrawn from consideration, and claims 18 to 31 were rejected. The claims now on appeal are claims 8, 18, 19, 26, 28, 29 and 31. Other claims 32 to 34 and revised original claims were presented in amendments dated December 5, 2001, and June 17, 2002 which were not entered.

(4) Status of amendments

Two amendments were filed subsequent to final rejection. The Examiner refused to enter the amendment filed December 5, 2001, and took no action on the second amendment filed June 17, 2002, which also was denied entry. Neither amendment was entered in part.

(5) Summary of invention

The present invention as defined in the appealed claims relates to wet processing of semiconductor wafers and more particularly to a special wafer cleaning system that is effective in removing sub 0.1-micron size particles that cannot be removed effectively by any known prior-art process. (page 6, lines 1-6)

The RCA-type wafer cleaning methods of Werner Kern that have been standard in the semiconductor industry for more than a quarter of a century have been improved substantially during the last decade by use of megasonic transducer means.

(page 6, lines 7-10) Improved megasonic cleaning means can remove particles as small as 0.15 micron. However, such wet cleaning techniques are not effective in removing extremely small sub 0.1-micron particles (e.g., those with a particle size from 0.01 to 0.07 micron). (page 6, lines 17-22)

Heretofore the semiconductor industry was convinced that wet cleaning methods would never be effective in removing such small contaminant particles. (page 6, lines 23-25) The best scientific minds grappling with the problem assumed, with good reason, that the tremendous van der Waals adhesive forces acting on very small or colloidal-size particles at the wafer surface could not be overcome and that elimination of such particles by a simple wet cleaning operation was virtually impossible. The experts were convinced that the only real hope for success was a breakthrough or major improvement in dry wafer cleaning technology, perhaps a sophisticated laser technique. A breakthrough or major discovery was considered essential if the industry was going to proceed with plans to reduce the feature size or minimum line width of the advanced microchips to 0.15 micron or less. (page 7, lines 1-11)

The present invention provides the needed breakthrough and eliminates the need for a drastic switch from the usual wet cleaning systems to a new dry system. It involves the amazing discovery that colloidal-size particles and sub 0.05-micron particles bonded to a wafer surface containing delicate microcircuits can easily be removed and repelled when the wafer is negatively charged in a suitable manner by applying a

relatively small or limited voltage, such as 10 to 40 volts or more, insufficient to damage or degrade vulnerable portions of the microcircuits or significantly reduce the yield of top-quality microchips (page 7, lines 12-22). The invention is really remarkable and a giant step forward in the art because sub 0.1-micron particles and colloidal particles can be effectively removed without the assistance of megasonic transducers (page 54, lines 12 to 15; page 56, lines 22 to 26).

In the semiconductor industry, one of the current target goals in microchip fabrication is to reduce the defect density to less than 0.03 defects per square centimeter. (page 5, Table 1) An object of the present invention is to reach that goal in a simple and effective manner by substantially eliminating "killer particles" (e.g., with a particle size in the range of from 0.03 to 0.09 micron) and minimizing the number of troublesome particles (e.g., those with a particle size more than 10 percent of the minimum line width or feature size) which are detrimental or highly undesirable. (page 10, lines 1-8)

The term "killer defect" is used herein in the broad sense to cover an unacceptable or intolerable defect in the microelectronic circuits of a semiconductor device or microchip caused by a contaminant particle trapped or embedded in the device during the fabrication process. (page 10, lines 9-13)

The term "killer defect" is used in a narrow sense in Table 1 on page 5 of this specification to describe trapped or embedded particles with a particle size that is at least about 20 percent of the minimum line width or feature size (identified

in the table as "Min. dimension"). That table from the SEMATECH road map indicates that one of the goals is to obtain a 90-percent yield of advanced (0.25 um) wafers with no more than 0.03 killer defects per square centimeter. (page 10, lines 17-24)

Particle removal in the sub 0.1 micron regime is a key requirement for advanced cleaning technologies and is essential when making modern microchips with a line width of 0.25 micron. Unfortunately megasonic cleaning technology is ineffective in removing silica particles of such small size.

The simple fact is that current wet cleaning technology does not provide the answer to the microcontamination problem and would not permit reduction in line widths to 0.13 micron or below, the industry goal.

The aforesaid 1993 Kern handbook confirms the inadequacy of wet cleaning technology and indicates that dry cleaning processes will have to be used in the future to obtain the ultrapurity needed for the next generation of microchips. (page 19, lines 16-28)

For the last 30 years the most competent scientists have been convinced that the primary force binding a colloidal-size particle to a wafer surface is van der Waals attraction which is universal and dominating when separation distances between a particle and a surface are extremely small (e.g., below 5 namometers). The forces of attraction increase as the particle size decreases so that it appears virtually impossible

to overcome the van der Waals forces when the particle size is 0.01 micron or less. (page 29, lines 21-29)

On this basis foremost experts, such as RCA's Werner Kern, concluded that wet cleaning processes could not provide a satisfactory way to remove sub 0.1-micron particles when manufacturing the most advanced microchips and that new dry methods would have to be developed. (page 30, lines 3-7)

Attempts were made to improve the effectiveness of wet wafer cleaning processes by causing strong or violent agitation of the liquid as by providing bursts of energy from megasonic transducers. However, such methods were not adequate for removal of sub 0.1-micron particles. Heretofore, more sophisticated dry cleaning methods seemed to provide the only real hope for minimizing particulate contamination when manufacturing advanced microprocessors with a minimum feature size or line width of 0.15 micron or less. (page 30, lines 8-18)

The unique wet wafer cleaning system of the present invention is a godsend to the semiconductor industry, which heretofore had no practical and effective way to eliminate "killer" particles of sub 0.1-micron size or to reach target defect-density goals, such as those set forth in Table 1 on page 5 of the present application. (page 59, lines 4-9)

In the practice of the invention, electrolysis and current flow must be avoided. Destructive electrolysis cannot occur when the semiconductor wafers are charged by <u>induction</u> as in the apparatus embodiments of the invention described in connection with Figures 1 to 12 of the drawings. As shown in

Figures 6 and 7, for example, a flat circular electrode or charge plate 10 with a diameter about the same as that of the semiconductor wafer w is mounted on the exterior surface of the glass receptacle A of Figure 2. During the wet cleaning operation, each silicon wafer is spaced from the electrode (10) and readily charged by induction (See page 42, lines 8 and 9; page 46, lines 12 to 16; and page 48, lines 1 to 9). The necessary electric charge on each wafer face is obtained by induction when a charged electrode is placed near the wafer as shown in the drawings (page 48, lines 1 to 9).

In the embodiment of the invention described in connection with Figure 12 of the drawings, a plurality of semiconductor wafers are cleaned in a water-filled tank or vessel. A row of from 10 to 20 or more silicon wafers immersed in an aqueous bath can be cleaned at one time in a tank or receptacle, such as one of the type shown in Figure 12 and described on page 8 (see lines 8 to 16).

The electrodes or charge plates (e.g., comparable to the charge plates 10) charge all of the wafers in the row by <u>induction</u> so that substantial electrolysis cannot occur in the bath. Charging the wafers by induction is an important advantage of appellant's invention because it precludes destructive electrolysis at the exposed conductor surfaces of the microelectronic circuits formed on the front face of each wafer (See page 46, lines 17 to 24).

In a preferred embodiment of the invention, an <u>induced</u> electric charge suitable for effective removal of sub 0.1-micron

contaminant particles is applied to each semiconductor wafer during batch-type wet processing operations in which 20 to 40 or more silicon wafers are treated simultaneously in a single wafer carrier or cassette (page 8, lines 8 to 16). This preferred embodiment as described in connection with Figure 12, for example, is specifically claimed in appealed claim 31.

If the wafer carrier contains a single row of 20 to 40 semiconductor wafers and is submerged in an aqueous bath in a tank or receptacle having a suitable external charge plate or electrode near and spaced from the outermost wafer at each end of the row, then all of the many wafers will be readily charged by induction to the desired voltage and field intensity. A wafer carrier or cassette of very simple construction can function remarkably well in the practice of the invention.

(6) Issues

(Issue One) The first issue is whether claims 8, 18, 26 and 28 are anticipated by Flitsch et al Patent No. 6,136,669 under 35 USC 102(e). In determining the basic differences between appellant's invention and the invention of that patent, a number of questions should be considered, including the following:

(a) Does the Flitsch et al patent have any relevance or probative value with respect to appellant's invention as claimed?

(b) Do the appealed claims define the invention in a clear and definite manner sufficient to distinguish from the disclosure of that patent?

(c) Does the subject matter disclosed in the Flitsch et al patent meet the terms of any claim?

(d) Would the corona discharge method or apparatus shown and described in that patent be operative or have any utility in the wet processing or wet cleaning of semiconductor or wafers?

(e) Does the bold final rejection of appellant's claims under 35 USC 102 have any rational basis or evidence thoughtful review and understanding of the different inventions disclosed by appellant and Flitsch et al and the particular problems to which they are directed?

(Issue Two) The second issue is whether claims 19, 29 and 31 can properly be rejected under 35 USC 103(a) as being unpatentable over the Flitsch et al patent in view of admitted prior art. This requires consideration of a number of questions, including the following:

(a) Does the prior art relied on in the rejection disclose or teach the subject matter and specific limitations set forth in the appealed claims?

(b) Does the prior art relied on in the rejection recognize and/or provide a practical solution to the particulate contamination problem solved by appellant's invention?

(c) Does the modification of the Flitsch et al process proposed in the rejection provide a useful or operative method for wet processing of silicon wafers or one that is effective in removing sub 0.1-micron "killer defects"?

(d) Does the prior art taken as a whole lead away from the invention?

(e) Is there a factual basis for rejection under 35 USC 103 including evidence of a motivating force that would cause a person skilled in the art to do what appellant has done?

(f) Does the Flitsch et al patent teach or suggest a practical method for wet cleaning semiconductor wafers 10 to 20 at a time as defined in claim 31?

(7) Grouping of Claims

Appellant contests the rejection of claims 8, 18, 26 and 28 as being anticipated under 35 USC 102. In that group of four claims, claim 8 is believed to be separately patentable and, therefore, does not stand or fall together with the other claims of the group.

Appellant also contests the rejection of claims 19, 29 and 31 for obviousness under 35 USC 103 based on admitted prior art. In that group of claims, claim 31 is believed to be separately patentable and does not stand or fall with the other claims of the group.

(8) Argument

All of the appealed claims 8, 18, 19, 26, 28, 29 and 31 were rejected as being anticipated or unpatentable based on a single patent which in fact has no relevance. It would be manifest to any competent person who reads and understands Flitsch et al Patent No, 6,136,669 that it has nothing to do with appellant's wet cleaning process or the removal of

particulate contaminants and that there is no legitimate issue in this case worthy of consideration by the Board.

(Issue One) The first issue relates to the rejection of claims 8, 18, 26 and 29 under 35 USC 102 as being anticipated by the Flitsch et al patent. As clearly explained hereinafter, the disclosure of that patent is irrelevant and immaterial and has no probative value with respect to the merits of appellant's invention. This type of evidence would be inadmissible in a court of law because it has no logical or rational relevance.

That patent relates to a dry process for removing highly mobile sodium ions from a silicon wafer, a problem which is easily solved when the wafer is heated above 400°F (e.g., 200° to 300°C) because of the mobility of the ions. That simple problem is unrelated to the difficult problem solved by appellant's wet wafer cleaning process, removing sub 0.1-micron "killer" particles that are so strongly bonded to the wafer surface that it is seemingly impossible to remove them. No scientist would seriously consider using the mobile-ion removal process of the Flitsch et al patent to remove particles bonded to the wafer face. That makes no sense and obviously could not remove such particles.

The problems caused by mobile ions are discussed in detail in the article by M. Kuhn entitled "Ionic Contamination and Transport of Mobile Ions in MOS Structure", J. Electrochem. Soc., vol. 118, p. 966 (1971). In the manufacture of semiconductor microelectronic devices, such as MOS integrated circuits, mobile sodium ions occur in the oxide layers of MOS

devices and are detrimental to device performance. In silicon field-effect transistors (FET), for example, sodium ions and other mobile ions in the gate oxide layer cause shifts in the operating voltage of the device as is well known in the art.

Flitsch Patent No. 6,136,669, the patent relied on by the Examiner in rejecting the appealed claims, discusses this problem at column 1, lines 20 to 24 and states "Over time, device operation causes mobile ions to move through the gate oxide layer causing operational device functional characteristic variations, such as device threshold voltage shifts, subthreshold leakage and impaired device isolation. Circuits with ion affected devices become unstable."

The purpose of the invention disclosed in the Flitsch patent is to improve semiconductor device stability by removal of mobile alkali ions contaminating the semiconductor chip oxide and insulating layers. This is accomplished by applying a corona discharge bias to the insulating layer that creates an electric charge opposite in polarity to the mobile ions of the insulating layer (See claim 1 of the patent).

As shown in figure 3A of the patent (after the gate oxidation step 100 of the flow diagram shown in Figure 2), a corona discharge gun of the type disclosed in Verkuil Patent No. 5,498,974 generates a corona bias which is directed to the semiconductor wafer 112 and creates an electric charge on the wafer surface. Step 102 of the Flitsch process (shown and described in Figure 2) is described at column 3, lines 64 to 66 as follows:

"The wafer 112, represented by device structure, is held on a wafer chuck, where it is subjected to bias-temperature conditions of -1MV/cm at 200°C to 300°C for 2 to 3 minutes."

Step 102 of Figure 2 is followed by step 104, a DI water rinse to remove both the corona charge and the mobile sodium ions.

Thus it is crystal clear that the electric charge is applied while the wafer is dry (Water has a boiling point of 100°C and cannot exist in the liquid phase at a temperature of 200°C or more).

The invention of Flitsch can be readily understood by carefully considering the drawings of his Patent No. 6,136,669 and the description thereof at column 1, lines 33 to 60, which is quoted below.

"FIGS. 1A-C show mobile ions being formed in a cross section of a semiconductor wafer during typical prior art semiconductor manufacturing steps, field effect transistor (FET) manufacturing steps in this example . . . A thin gate oxide layer 56 is formed over the semiconductor layer 50."

"FIG. 1B is an expanded view at a typical device region 52. In the expanded view of FIG. 1B, mobile ions 58 (Q_m) are trapped in the thick insulator 54 and thin gate oxide 56. In this example, the mobile ions 58 are primarily positively charged ions, and primarily at the semiconductor-isolator interface (e.g., the oxide-silicon interface). . . . Mobile ions 58 remain in the structure as a result of prior processing steps."

"In FIG. 1C, a gate 60 (e.g., polysilicon), is formed on the structure of FIG. 1B."

"Under normal device operation, bias voltages on the gate 60 eventually force the mobile ions 58 through the gate oxide 5 6'. The movement of these mobile ions 58 alters the FET's threshold voltage (V_T), making the FET unstable, in effect, giving the FET a time varying V_T."

The undesirable sodium ions on a semiconductor wafer are highly mobile and easy to remove when the dry wafer is heated above 400°F (e.g., to a temperature of from 200°C to 300°C as in the Flitsch patent. A "killer" particle (or "killer defect" as defined at page 10, lines 17-24) having a particle size of 0.02 to 0.05 micron, for example, is bonded to the wafer surface and seemingly impossible to remove because of the tremendous van der Waals forces described at page 29, lines 21-29.

The simple fact is that sodium ions do not become bonded to a wafer surface like sub 0.1-micron particles but are highly mobile and easy to remove. The problems of ionic contamination and particulate contamination are substantially unrelated and nonanalogous. The Flitsch patent is concerned with mobile alkali ions, not sub 0.1-micron particles, and is in no way pertinent to the appealed claims which require application of an electric charge to the wafer face during wet processing while the wafer is wet (e.g., below 220°F) rather than dry or at a temperature above 400°F as in Flitsch.

It is manifest that there is no legitimate or bona fide issue in this case requiring consideration by the Board of Appeals because all of the rejections are based on the same irrelevant patent that has no probative value.

The limited scope of the claims

The Examiner has boldly rejected most of the appealed claims as being anticipated under 35 USC 102, apparently contending that the claims fail to include temperature limitations or other limitations sufficient to distinguish from Flitsch patent No. 6,136,669. That rejection and the associated construction of the claims are manifestly erroneous. The appealed claims are clear and definite and use terms such as "wet processing", "particulate" and "particle", whose meanings could not be misunderstood by persons familiar with the art.

The meaning of "wet"

As pointed out at pages 3 and 31 of the specification, the terminology used should be construed as consistent with authoritative textbooks, such as "Handbook of Semiconductor Wafer Cleaning Technology" by Werner Kern (1993).

Pages 201 and 203 of Kern's 1993 handbook indicates that there are two types of wafer cleaning processes in commercial use. They are liquid phase, or wet, wafer cleaning processes and gas-phase, or dry, wafer cleaning processes. The vast majority are wet processes. As stated "In general, it is not expected that dry cleaning will replace wet cleaning . . . much needs to be accomplished to make it [dry cleaning] fully compatible with large scale industrial production." Today, wet

wafer cleaning is the most frequently applied processing step in microchip fabrication. Dry cleaning is seldom used and is not needed and not used in the typical 360-step manufacturing process described on pages B-3 to B-14 of the SEMATECH publication referred to on page 3 of this application.

The word "wet" has become a well-established term of art whose meaning is unmistakable. In Flitsch Patent No. 6,136,669, for example, there can be no problem determining the meaning of "wet chemical process steps" (col. 1, line 27), "wet step" (col. 3, line 19; col. 4, line 33), "wet wafer preclean" (col. 4, line 36) or "wet process step" (col. 6, line 24).

The term "wet" is also a temperature limitation because water (b.p. 100°C) or an aqueous liquid cannot remain in the liquid state at a temperature substantially above the boiling point. In the Flitsch patent the corona charge is applied to a dry wafer at a temperature of 200°C before the subsequent water rinse. Column 3, lines 15 to 20 of the patent, indicates that the corona bias-temperature step to remove mobile [sodium] ions is carried out before proceeding with a wet step. The invention as defined in the appealed claims requires applying an electric charge to the wafer face during (not before) the wet processing step. The Flitsch patent is substantially nonanalogous and in no way pertinent to the claimed invention. The 35 USC 102 "anticipation" rejection based on Flitsch makes no sense.

The meaning of "particle"

The word "particulates" has also become a well-established term of art and is clearly defined in the Van Zant textbook "Microchip Fabrication" (Second Edition) referred to on page 3 of the present application. Pertinent portions from page 146 of that textbook are quoted below.

"Wafer surfaces can have four different types of contamination . . . The four types are

1. Particulates
2. Organic residues
3. Inorganic residues
4. Unwanted oxide layers

"Particulates on the wafer surface vary from large ones (50-micron size) to very strong ones about a micron in size . . . The smaller particulates are more difficult to remove because they are held to the surface by strong intermolecular forces."

"Particulates" is a term of art concerned with solid particles and in no way includes subatomic particles or mobile ions of the type described in the Flitsch patent. It is manifest that the term "particulate" as used, for example, in original claims 7 and 21 and defined on pages 24 and 25 of the specification and the term "killer particles" or "killer defect" as used, for example, in original claim 8 and defined at pages 4, 5 and 10 of the specification, relate to solid particles, not ions.

It is also clear that the term "particle" is used in the present application in the normal sense as customarily used in the semiconductor industry in connection with particulate contamination. A mobile ion, such as a sodium ion can in no way

be considered a "particle" as that term is used in the specification and claims of the present application. In the field of wafer fabrication and wafer cleaning, the terms "particles" and "particulates" are, of course, synonymous.

The appealed claims are definite and clearly distinguish from ions or mobile ions by reference to particles. Claim 8 refers to "submicron killer particles bonded to the front face of the wafer". Claims 18 and 19 are limited to "sub 0.1 micron contaminant particles bonded to the wafer surface". Claim 26 recites "sub 0.1-micron particles bonded at the wafer face". Claim 29 refers to "effective removal of sub 0.05-micron particles that are strongly bonded to the wafer face". Prior to the present invention, effective removal of killer particles in the size range of 0.02 to 0.05 microns was considered virtually impossible with known technology. Appellant's invention is of a pioneer nature.

It is manifest that the subject matter disclosed in Flitsch et al Patent No. 6,136,669 is not pertinent and does not meet the terms of any of the appealed claims. Claim 8 defines a wet cleaning process wherein the semiconductor wafer is rinsed in DI [ultrapure deionized] water and "the wafer is charged during rinsing to a voltage of at least 100 volts." Claim 18 and related dependent claims 19 and 31 define a wet wafer cleaning process in which the "front face of the process wafer is artificially charged during wet processing." In the process of claim 19 the wafer is "subjected to chemical cleaning and DI

rinsing operations while said front face is negatively charged."

Claim 29 is specific and states that "the wafer surface . . . is electrically charged during the wet cleaning process to cause effective removal of sub 0.05-micron particles."

Claims 26 and 28 define a process for manufacture of advanced microchips in which many wet cleaning operations are employed to remove the contaminant particles and the wafer face is electrically charged during the cleaning operations to remove sub 0.1-micron particles. The electric charge is provided "during most of said wet cleaning steps to minimize particulate contamination" (claim 28, lines 3 and 4).

The patent to Flitsch et al is not pertinent and uses corona discharge means to apply an electric charge to a dry (not wet) wafer heated to a temperature above 400°F (e.g., 200° to 300°C) as indicated in Figure 2 of the patent in claim 4, in the abstract, and in the specification (column 3, line 66; column 4, lines 12 to 16). The patent relates to the removal of highly mobile ions and has nothing to do with the removal of minute (immobile) particles strongly bonded to the wafer surface, such as those in the "killer" size range of from 0.02 to 0.07 microns.

It is readily apparent that there is no basis whatsoever for the rejection of claims 8, 18, 26 and 28 as being anticipated under 35 USC 102. It is believed that claim 8 is separately patentable and does not stand or fall with claims 18,

26 and 28 because it is more specific than those claims and is directed to a different species of the invention wherein the wafer is charged during rinsing in pure deionized (DI) water to a voltage of at least 100 volts. It is manifestly impossible, using the corona discharge method of the Flitsch et al patent, to apply such a high voltage to a wet semiconductor wafer during a water rinse as required in claim 8.

Operativeness -- Corona bias in water

A person skilled in the art who read the Flitsch et al patent would know that the corona discharge method of that patent is completely inoperative and has no utility in the wet processing or wet cleaning of semiconductor wafers. This should be manifest to anyone from the drawings, the abstract, and the specification of that patent.

The Abstract states that the surface mobile ions are removed with a deionized (DI) water rinse or a standard wet cleaning step. In the drawings, sheet 2 of 8, box 102 shows a corona discharge for 2 to 3 minutes at 200° to 300 °C and box 104 shows the subsequent DI wafer rinse.

The Flitsch specification (column 3, lines 16 to 24) points out that the (dry) corona bias-temperature step is completed before proceeding with a wet step and that such corona bias step draws mobile ions to the surface while the subsequent wet step removes the surfaced mobile ions. Column 4, lines 10 to 12, indicate the importance of high temperature by stating that the alkali ions are "still not readily mobile until the wafer 112 is heated above 200°C (i.e., above 400°F). As stated

at lines 24 and 25 "After drawing ions to the oxide surface . . . the surface corona charge is removed." The paragraph at lines 34 to 40 of column 4 of the Flitsch et al patent explains how the electric corona charge is removed or destroyed when the wafer is washed with a deionized (DI) water rinse or a standard wet wafer cleaning step.

In other words, the corona bias charge on the dry wafer (applied while the wafer is heated above 400°F) is immediately destroyed when the wafer is wetted or washed in water or an aqueous liquid. It is therefore impossible to apply an electric corona charge to a wet wafer by the process of Flitsch et al. That patent is inoperative and irrelevant with respect to a wet wafer cleaning system of the type described in the appealed claims.

The bold final rejection of appellant's claims under 35 USC 102 has no rational basis. That hasty and ill-advised rejection is unworthy, whether due to an innocent illusion, overconfidence, superficial consideration of the Flitsch et al disclosure, or lack of familiarity with the technology, and seems to evidence a lack of understanding or appreciation of the pioneer nature of the invention or its importance in the manufacture of the most advanced microchips having feature sizes or line widths of 0.15 micron or less.

(Issue Two) The second issue relates to the rejection of claims 19, 29 and 31 for obviousness under 35 USC 103 and is to a great extent the same as Issue One because the rejection is based almost entirely on the Examiner's mistaken belief that the

basic invention is fully anticipated by Flitsch et al Patent No. 6,136,669. In essence the rejection of dependent claims 19 and 31 as set forth by the Examiner is that they differ from their fully anticipated base claim 18 by reciting matter that is quite obvious from admitted common practice in the prior art.

In other words, the basic reason for the rejection of claims 19 and 29 under 35 USC 103 is that they add nothing unobvious or patentably significant to the subject matter of the four claims rejected as being fully anticipated by the Flitsch et al patent. That rejection is not based on any contention that appellant's novel combination and the fundamental features of the claimed invention would be obvious from a logical combination of prior art references. Instead the rejection of these claims under 35 USC 103, as set forth by the Examiner, assumes that the fundamental combination is fully disclosed in the Flitsch patent and is based on a finding that the added features recited in these claims are obvious, incidental and/or matters of common practice.

As stated in the final Office action, the claims were "rejected under 35 USC 103(a) as being unpatentable over Flitsch et al. as applied to claim 1 above in view of Applicant's admitted prior art . . . common practice in the industry." In the rejection of claim 1 as being anticipated, it is stated "Flitsch et al. teach a method of removing ions from the surface of a wafer using direct current source during wet processing;" This is totally false and a major, major mistake which clearly invalidates all of the rejections in the present case.

The indisputable fact is that the disclosure of the Flitsch et al patent relied on by the Examiner in the rejection under 35 USC 103 does not meet the terms of any of the appealed claims. That was pointed out previously in some detail. Claims 19, 29 and 31 clearly distinguish from the Flitsch disclosure by requiring electrical charging of the wafer face during wet processing to cause effective removal of sub 0.05-micron particles bonded to the wafer surface.

The Flitsch et al patent has nothing to do with the particulate contamination problem solved by appellant's invention. The examiner has not cited or relied on any prior art reference that remotely suggests that invention or a practical solution to that problem. The simple fact is that there is no known wafer cleaning process in the prior art capable of eliminating sub 0.05-micron killer particles during processing of semiconductor wafers.

It would appear that the Examiner's rejections are based on the delusion that the Flitsch et al patent discloses a satisfactory and operative method for removing sub 0.1-micron killer particles from semiconductor wafers. The truth is that the corona discharge equipment and corona-bias method of that patent is suitable for removing mobile sodium ions from a wafer heated to a temperature above 400°F. (e.g., 200° to 300°C) but cannot dislodge or remove submicron particles bonded to the wafer surface. The Flitsch corona-bias method has no utility in wet processing operations and would be completely inoperative and unable to apply an electric charge to a wet wafer if an

attempt were made to apply such a charge during a water rinse or any other wet cleaning or wet processing operation. Simply put, the corona discharge means of Flitsch is manifestly inoperative in water and was never intended to be used on a wet wafer.

One of the elementary principles of patent law has apparently been ignored in the present case. A narrow hindsight focus on one or two prior art patents in a vacuum is not realistic and not a proper basis for rejection when the prior art taken as a whole leads away from the claimed invention. That is particularly true when speculating as to the possible significance of an obscure patent with insufficient disclosure or a patent with a specification which tends to confuse or is not understood, such as the misconstrued Flitsch et al patent.

In the present case the prior art as a whole leads away from appellant's invention. The most reliable evidence was published by foremost experts in the wafer cleaning field, such as Werner Kern, the father of the standard RCA wet clean system used for the last 30 years in almost all microchip fabrication plants in the world. His 1998 textbook "Handbook of Semiconductor Wafer Cleaning" (680 pages), referred to on page 3 of appellant's specification, is required reading for anyone active in the field and should not be overlooked when evaluating appellant's invention. As pointed out at page 30, lines 3 to 7, of the specification, Werner Kern concluded that wet wafer cleaning processes could not provide a satisfactory solution to the problem of sub 0.1-micron killer defects and that the only real hope was to develop a new <u>dry</u> wafer cleaning process. Mr.

Kern and the other foremost experts in wafer cleaning technology were convinced that it would be virtually impossible to remove colloidal-size particles because of the van der Waals forces (page 29, lines 21-29). However, appellant showed they were wrong and made a remarkable discovery that is not remotely suggested by the prior art. The prior art as a whole does not suggest or in any way contemplate appellant's invention.

The Examiner has failed to provide any factual basis for his rejection under 35 USC 103 and has produced no evidence of an obvious reason or a motivating force that could lead to appellant's invention. The law places a heavy burden on the PTO to justify the rejection of a patent claim.

The burden is on the Commissioner to establish that the applicant is not entitled to a patent. The Patent Office is required to produce the factual basis for its rejection of patent claims under 35 USC 102 or 103 (In re Warner, 379 F2d 1011, 1016, 154 USPQ 173,177; Graham v. John Deere, 383 US 1, 148 USPQ 459). This includes the provision of evidence of a motivating force which would impel a person skilled in the art to do what applicant has done.

The examiner has produced no prior art that could justify his failure to allow claim 31, for example. There is nothing in the Flitsch et al patent that would motivate or lead a person to clean semiconductor wafers in the manner specified in that claim (e.g., 20 or more at a time in a wafer carrier). Claim 31 is very specific and is believed to be separately

patentable. That claim should not stand or fall with broader claims, such as claims 19 and 29.

There is no rational basis for arguing that the corona discharge method of the Flitsch et al patent is in any way pertinent with respect to claim 31. The process of claim 31 is inoperative and has no utility in the absence of water. A corona gun as disclosed in the Flitsch patent cannot apply a charge to each of the 10 to 20 or more silicon wafers in a row. Where would the gun be located? How could it possibly work under water or even in the absence of water?

Claim 31 is dependent on appealed claim 18 which defines a microchip fabrication process wherein the semiconductor wafer is "charged during wet processing to provide an effective field intensity . . . sufficient to facilitate removal of harmful sub 0.05-micron particulates bonded to the wafer surface."

Claim 31 is more specific than base claim 18 in defining a wafer fabrication process "wherein a row of 10 or more silicon wafers is supported in a vessel or wafer carrier" during the wet cleaning operations. This feature of the wet cleaning operation has astounding ramifications and advantages. Killer particles in the dangerous size range of 0.03 to 0.1 microns can be readily eliminated in a simple mass production system wherein a row of 20 to 30 or more parallel closely-spaced wet silicon wafers of large diameter are cleaned simultaneously in an aqueous liquid and are uniformly charged by induction to avoid harmful electrolysis. This unique combination is a

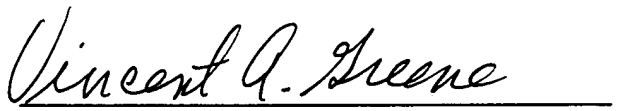
godsend to the semiconductor industry and not remotely suggested by the prior art. Heretofore, the industry had no practical method for eliminating sub 0.1-micron particulate contaminants (e.g., "killer defects") in the manufacture of advanced microchips. Applicant's solution to the problem is astounding because it is simple, inexpensive and remarkably effective. It is a pioneer invention in spite of its simplicity in retrospect. As stated by America's foremost patent jurist, Learned Hand "It is the obvious, put to use, that most often proves invention."

Appellant's invention solves a major problem in the semiconductor industry and is certainly worthy of patent protection. All of the appealed claims meet the novelty and inventive step requirements for patentability. It is manifest that the prior art of record fails to teach the method of cleaning a semiconductor wafer by applying an electric charge to the surface of the wafer during wet processing, such that particles less than 0.05 micron in size are effectively removed (** See footnote) with or without the assistance of megasonic transducer means (as specifically disclosed at the bottom of page 56 of the specification). The use of megasonic transducers or megasonic energy is optional and sometimes appropriate or advantageous (as indicated at page 8, lines 17 to 23; page 34, lines 12 to 16; and page 41, lines 5 to 10) "but is not necessary when employing the electropurge process of the present invention" (as stated at page 54, lines 12 to 15).

** See page 47, lines 20 to 27.

For the reasons set forth in this brief, the rejections of the appealed claims are clearly erroneous and should be overruled.

Respectfully submitted,



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August 16, 2002

APPENDIX

This appeal is taken from the rejection of eight claims which the applicant proposes to contest, copies of which are set forth below.

8. A wet cleaning process wherein a semiconductor wafer is cleaned by thorough rinsing in DI water characterized in that the wafer is charged during rinsing to a voltage of at least 100 volts in such manner that colloidal-size and submicron killer particles bonded to the front face of the wafer containing the delicate microcircuits are effectively removed or eliminated.

18. A process for fabrication of microelectronic devices on silicon wafers wherein microcircuits are formed on the front face of a wafer by a plurality of layering, patterning, doping and heating operations and the wafer is wetted and repeatedly subjected to cleaning, rinsing and drying operations to remove contaminants, characterized in that said front face of the process wafer is artificially charged during wet processing with a negative voltage of at least 2 volts sufficient to facilitate removal of sub 0.1 micron contaminant particles bonded to the wafer surface during the wet cleaning operations.

19. A process according to claim 18 wherein the front face of the process wafer is subjected to wet CMP polishing with colloidal silica or alumina particles having an average particle size of from 0.01 to 0.03 microns and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to cause efficient

or substantially complete removal of sub 0.05-micron contaminant particles bonded to the wafer surface.

26. In the manufacture of advanced microchips, a process for forming delicate microcircuits on the flat face of a semiconductor wafer in which the wafer is subjected to a large number of layering, patterning and doping operations and many wet cleaning steps with acid and alkaline solutions and pure water to remove intolerable contaminants, characterized in that the wafer face containing said microcircuits is electrically charged to a limited voltage of at least 2 volts to provide an effective field intensity that causes sub 0.1 micron particles bonded at the wafer face to be released and removed.

28. A process according to claim 26 wherein said wafer face is provided with a limited electric charge of at least 10 volts during most of said wet cleaning steps to minimize particulate contamination.

29. In the manufacture of advanced microchips from flat semiconductor wafers having delicate microcircuits formed on one face, an RCA-type wet cleaning process wherein a single wafer is treated in an aqueous alkaline solution containing hydrogen peroxide and thereafter treated in an acidic solution, rinsed in pure water and dried, characterized in that the wafer surface containing said delicate microcircuits is electrically charged during the wet cleaning process to cause effective removal of sub 0.05-micron particles that are strongly bonded to the wafer face.

31. A process according to claim 18 wherein a row of 10 or more silicon wafers is supported in a vessel or wafer carrier

during the cleaning operations, the front face of each wafer being charged to a limited negative voltage, such as 2 to 60 volts, insufficient to harm the delicate microcircuits formed on that face and having a field intensity of at least 0.02 volts/mm sufficient to cause efficient removal of harmful sub 0.05-micron particles.

5

Overview of Dry Wafer Cleaning Processes

Jerzy Ruzyllo

1.0 INTRODUCTION

-32-

Semiconductor wafer cleaning is the most frequently applied processing step in the IC manufacturing sequence. Therefore, both production yield and device performance depend to a significant extent on the quality of wafer cleaning methods employed. The commonly used technology of liquid-phase, or wet, wafer cleaning, discussed in detail in previous chapters, will certainly remain the workhorse of everyday IC processing, and advances in this area are needed and will be made. On the other hand, wet cleaning technology has a number of inherent shortcomings that may limit its effectiveness in the fabrication of at least some future generation integrated circuits. The need thus exists to replace this type of wafer cleaning in selected applications in high-end silicon IC manufacturing, such as next generation DRAMs (1), with equally effective gas-phase, or dry, wafer cleaning processes. During the last five years, impressive strides have brought dry wafer cleaning technology closer to industrial applications. Still, much needs to be accomplished to make it fully compatible with large scale industrial production.

Part III of this volume is devoted to dry semiconductor wafer cleaning processes, primarily addressing silicon technology. Authors of consecutive chapters detail important issues related to this emerging technology and discuss specific approaches proposed and investigated.

The purpose of this introductory chapter is to give an overview of dry wafer cleaning processes established to date. The reasons why "dry"

3.0 ANTICIPATED ROLE OF DRY WAFER CLEANING IN IC FABRICATION

The general discussion on the role of dry wafer cleaning operations in IC manufacturing should begin by stating that wafer cleans, although they account for a major part of all operations performed on the wafer, do not serve any constructive purpose. In other words, in contrast to oxidation, CVD, implantation, or etching, we do not need cleaning directly to build device features. We use it only because the wafer surface becomes contaminated in the course of the manufacturing process.

If liquids, resists, equipment, wafer handling utensils, and the process environment in general would not shed contaminants, then there would be no need for wafer cleaning. One may conclude from such reasoning that an ultimate goal in IC manufacturing technology should be a totally "cleaning-less" fabrication process. Following this reasoning, one may see dry cleaning methods playing an important role in bridging the IC technology of today with totally integrated "cleaning-less" technology of the future in which surface treatments will be limited only to processes such as native oxide removal, or surface passivation through oxidation or hydrogenation. It is in this context that both short term and long term roles of gas-phase processes in wafer cleaning technology should be considered.

In general, it is not expected that dry cleaning will replace wet cleaning applications in which the latter is successfully used. Instead, dry cleaning should be considered for those applications in which wet cleaning, due to its inherent limitations, cannot be used. First and foremost, this concerns in situ cleaning operations carried out within the integrated processor systems. An example of the likely early application of dry cleaning in cluster tool manufacturing is shown in Fig. 1. It is concerned with a three-step process for gate structure formation in MOS technology. Other likely applications, some of them already in place for some time, involve cleaning operations applied in two-step integrated processes including pre-contact cleans, pre-epi cleans, and cleans applied prior to polysilicon emitter formation in bipolar technology (4).

Overall, it can be assumed that during the next few years newly developed dry cleaning modules will be used predominantly in conjunction with clusters tool. It remains to be seen whether further refinements of dry cleaning methods will eventually lead to the use of dry cleaning reactors in the stand alone mode.

In further defining the potential role of dry cleaning in IC processing, one should also consider the ability of both dry and wet cleans to remove